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L2	95685	"712"/("20,21,22").ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 15:53
L3	210853	"345"/("606,607,608,609,610").ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 15:54
L4	210853	"345"/("501,502,503,504,505,506,519,520,522").ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 15:55
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L6	295351	2 or 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 15:55
L7	10965	surface adj region?	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 15:58
L8	777	6 and 7	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 15:55
L9	11112	((surface adj region?) or ((2D adj region) or (2D-region)) or ((3D adj region) or (3D-region)) with (size or sizing) with (reduc$3 or adjust$3 or modif$7))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 15:56
L10	804	6 and 9	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 15:56
L11	646	(first adj operand with second adj operand) with instruction	US-PGPUB; USPAT	OR	ON	2005/07/09 16:02
L12	0	(8 or 10) and 11	US-PGPUB; USPAT	OR	ON	2005/07/09 15:57
L13	209	6 and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 15:58
L14	0	7 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 15:58

L15	660892	region?	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 15:58
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L18	16	16 and 17	US-PGPUB; USPAT	OR	ON	2005/07/09 16:01
L19	562	7 and 5	US-PGPUB; USPAT	OR	ON	2005/07/09 16:01
L20	0	11 and 19	US-PGPUB; USPAT	OR	ON	2005/07/09 16:01
L21	19	(first adj operand with second adj operand) with instruction with parallel	US-PGPUB; USPAT	OR	ON	2005/07/09 16:03
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L24	1	22 and 23	US-PGPUB; USPAT	OR	ON	2005/07/09 16:03
L25	14	("4051551" | "4811210" | "4891751" | "4907148" | "4975843" | "5038386" | "5193202" | "5524223" | "5692210" | "5781195" | "5794016" | "6266733" | "6460127" | "6532017").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/09 16:06
L26	29754	operand	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:06
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Terms used simd and surface computer

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1 Rapid evaluation of Catmull-Clark subdivision surfaces
Jeffrey Bolz, Peter Schröder
February 2002 **Proceeding of the seventh international conference on 3D Web technology**
Full text available: pdf(910.23 KB) Additional Information: full citation, abstract, references, citings, index terms

Using subdivision as a basic primitive for the construction of arbitrary topology, smooth, free-form surfaces is attractive for content destined for display on devices with greatly varying rendering performance. Subdivision naturally supports level of detail rendering and powerful compression algorithms. While the underlying algorithms are conceptually simple it is difficult to implement player engines which achieve optimal performance on modern CPUs such as the Intel Pentium family.In this pape ...

2 The Reyes image rendering architecture
Robert L. Cook, Loren Carpenter, Edwin Catmull
August 1987 **ACM SIGGRAPH Computer Graphics , Proceedings of the 14th annual conference on Computer graphics and interactive techniques**, Volume 21 Issue 4
Full text available: pdf(944.35 KB) Additional Information: full citation, abstract, references, citings, index terms

An architecture is presented for fast high-quality rendering of complex images. All objects are reduced to common world-space geometric entities called micropolygons, and all of the shading and visibility calculations operate on these micropolygons. Each type of calculation is performed in a coordinate system that is natural for that type of calculation. Micropolygons are created and textured in the local coordinate sysem of the object, with the result that texture filtering is simplified and im ...

3 Real-time rendering: Interactive ray tracing of free-form surfaces
Carsten Benthin, Ingo Wald, Philipp Slusallek
November 2004 **Proceedings of the 3rd international conference on Computer graphics, virtual reality, visualisation and interaction in Africa**
Full text available: pdf(267.91 KB) Additional Information: full citation, abstract, references, index terms

Even though the speed of software ray tracing has recently been increased to interactive performance even on standard PCs, these systems usually only supported triangles as geometric primitives. Directly handling free-form surfaces such as spline or subdivision surfaces instead of first tesselating them offers many advantages such as higher precision results, reduced memory requirements, and faster preprocessing due to less primitives. However, existing algorithms for ray tracing free-form su ...

4 An updated cross-indexed guide to the ray-tracing literature
L. Richard Speer
January 1992 **ACM SIGGRAPH Computer Graphics**, Volume 26 Issue 1
Full text available: pdf(2.94 MB) Additional Information: full citation, index terms

5 Polygon rendering on a stream architecture
John D. Owens, William J. Dally, Ujval J. Kapasi, Scott Rixner, Peter Mattson, Ben Mowery
August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Full text available: pdf(161.65 KB) Additional Information: full citation, abstract, references, citings, index terms

The use of a programmable stream architecture in polygon rendering provides a powerful mechanism to address the high performance needs of today's complex scenes as well as the need for flexibility and programmability in the polygon rendering pipeline. We describe how a polygon rendering pipeline maps into data streams and kernels that operate on streams, and how this mapping is used to implement the polgyon rendering pipeline on Imagine, a programmable stream processor. We compare our resul ...

Keywords: OpenGL, SIMD, graphics hardware, kernels, media processors, polygon rendering, stream architecture, stream processing, streams

6 Variable-precision rendering
Xuejun Hao, Amitabh Varshney
March 2001 **Proceedings of the 2001 symposium on Interactive 3D graphics**
Full text available: pdf(8.33 MB) Additional Information: full citation, references, index terms

Keywords: hierarchical rendering, levels of detail, variable-precision rendering, view-dependent rendering

7 Approximation & refinement: Data-dependent fairing of subdivision surfaces
Ilja Friedel, Patrick Mullen, Peter Schröder
June 2003 **Proceedings of the eighth ACM symposium on Solid modeling and applications**
Full text available: pdf(945.44 KB) Additional Information: full citation, abstract, references, index terms

In this paper we present a new algorithm for solving the data dependent fairing problem for subdivision surfaces, using Catmull-Clark surfaces as an example. Earlier approaches to subdivision surface fairing encountered problems with singularities in the parametrization of the surface. We address these issues through the use of the characteristic map parametrization, leading to well defined membrane and bending energies even at irregular vertices. Combining this approach with ideas from data-dep ...

Keywords: CAD, Catmull-Clark, bicubic b-splines, fairing, geometric modeling, nonlinear minimization, subdivision surfaces, thinplate energy

8 A language for shading and lighting calculations
Pat Hanrahan, Jim Lawson
September 1990 **ACM SIGGRAPH Computer Graphics , Proceedings of the 17th annual conference on Computer graphics and interactive techniques**, Volume 24 Issue 4
Full text available: pdf(2.08 MB) Additional Information: full citation, abstract, references, citings, index terms

A shading language provides a means to extend the shading and lighting formulae used by a rendering system. This paper discusses the design of a new shading language based on previous work of Cook and Perlin. This language has various types of shaders for light sources and surface reflectances, point and color data types, control flow constructs that support the casting of outgoing and the integration of incident light, a clearly specified interface to the rendering system using global state var ...

9 Pixel-planes 5: a heterogeneous multiprocessor graphics system using processor-enhanced memories
Henry Fuchs, John Poulton, John Eyles, Trey Greer, Jack Goldfeather, David Ellsworth, Steve Molnar, Greg Turk, Brice Tebbs, Laura Israel
July 1989 **ACM SIGGRAPH Computer Graphics , Proceedings of the 16th annual conference on Computer graphics and interactive techniques**, Volume 23 Issue 3
Full text available: pdf(2.01 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper introduces the architecture and initial algorithms for Pixel-Planes 5, a heterogeneous multi-computer designed both for high-speed polygon and sphere rendering (1M Phong-shaded triangles/second) and for supporting algorithm and application research in interactive 3D graphics. Techniques are described for volume rendering at multiple frames per second, font generation directly from conic spline descriptions, and rapid calculation of radiosity form-factors. The hardware consists of up t ...

10 Extracting iso-valued features in 4-dimensional scalar fields
Chris Weigle, David C. Banks
October 1998 **Proceedings of the 1998 IEEE symposium on Volume visualization**
Full text available: pdf(621.93 KB) Additional Information: full citation, references, citings, index terms

11 Real-time procedural textures
John Rhoades, Greg Turk, Andrew Bell, Andrei State, Ulrich Neumann, Amitabh Varshney
June 1992 **Proceedings of the 1992 symposium on Interactive 3D graphics**
Full text available: pdf(1.61 MB) Additional Information: full citation, references, citings, index terms

Illuminating micro geometry based on precomputed visibility

Wolfgang Heidrich, Katja Daubert, Jan Kautz, Hans-Peter Seidel

July 2000 **Proceedings of the 27th annual conference on Computer graphics and interactive techniques**

Full text available: pdf(4.35 MB) Additional Information: full citation, abstract, references, citings, index terms

Many researchers have been arguing that geometry, bump maps, and BRDFs present a hierarchy of detail that should be exploited for efficient rendering purposes. In practice however, this is often not possible due to inconsistencies in the illumination for these different levels of detail. For example, while bump map rendering often only considers direct illumination and no shadows, geometry-based rendering and BRDFs will mostly also respect shadowing effects, and in many cases even indirect ...

Keywords: Monte Carlo techniques, frame buffer tricks, graphics hardware, illuminatiion effects, reflectance & shading models, texture mapping

13 Generating textures on arbitrary surfaces using reaction-diffusion

Greg Turk

July 1991 **ACM SIGGRAPH Computer Graphics , Proceedings of the 18th annual conference on Computer graphics and interactive techniques**, Volume 25 Issue 4

Full text available: pdf(6.01 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a biologically motivated method of texture synthesis called *reaction-diffusion* and demonstrates how these textures can be generated in a manner that directly matches the geometry of a given surface. Reaction-diffusion is a process in which two or more chemicals diffuse at unequal rates over a surface and react with one another to form stable patterns such as spots and stripes. Biologists and mathematicians have explored the patterns made by several reaction-diffusion ...

Keywords: biological models, reaction-diffusion, texture mapping

14 Perlin noise pixel shaders

John C. Hart

August 2001 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(919.41 KB) Additional Information: full citation, abstract, references, citings, index terms

While working on a method for supporting real-time procedural solid texturing, we developed a general purpose multipass pixel shader to generate the Perlin noise function. We implemented this algorithm on SGI workstations using accelerated OpenGL PixelMap and PixelTransfer operations, achieving a rate of 2.5 Hz for a 256x256 image. We also implemented the noise algorithm on the NVidia GeForce2 using register combiners. Our register combiner implementation required 375 passes, but ran at 1.3 H ...

Keywords: Perlin noise function, hardware shading, pixel shaders, register combiners

15 Scalable parallel algorithms for interactive visualization of curved surfaces

Subodh Kumar, Chun-Fa Chang, Dinesh Manocha

November 1996 **Proceedings of the 1996 ACM/IEEE conference on Supercomputing (CDROM) - Volume 00**

Full text available: pdf(972.57 KB) Additional Information: full citation, abstract, references, citings

We present efficient parallel algorithms for interactive display of higher order surfaces on current graphics systems. At each frame, these algorithms approximate the surface by polygons and rasterize them over the graphics pipeline. The time for polygon generation for each surface primitive varies between successive frames and we address issues in distributing the load across processors for different environments. This includes algorithms to statically distribute the primitives to reduce d ...

Keywords: Surface tessellation, Load balancing, Real-time rendering, Simulation-based Design, Splines

16 Motions & transformations: Fast swept volume approximation of complex polyhedral models

Young J. Kim, Gokul Varadhan, Ming C. Lin, Dinesh Manocha

June 2003 **Proceedings of the eighth ACM symposium on Solid modeling and applications**

Full text available: pdf(3.66 MB) Additional Information: full citation, abstract, references, index terms

We present an efficient algorithm to approximate the swept volume (SV) of a complex polyhedron along a given trajectory. Given the boundary description of the polyhedron and a path specified as a parametric curve, our algorithm enumerates a superset of the boundary surfaces of SV. It consists of ruled and developable surface primitives, and the SV corresponds to the *outer boundary* of their arrangement. We approximate this boundary by using a five-stage pipeline. This includes computing a ...

Keywords: distance fields, implicit modeling, swept volume

17 A radar simulation program for a 1024-processor hypercube
J. L. Gustafson, R. E. Benner, M. P. Sears, T. D. Sullivan
August 1989 **Proceedings of the 1989 ACM/IEEE conference on Supercomputing**
Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, references, citings, index terms

We have developed a fast parallel version of an existing synthetic aperture radar (SAR) simulation program, SRIM. On a 1024-processor NCUBE hypercube it runs an order of magnitude faster than on a CRAY X-MP or CRAY Y-MP processor. This speed advantage is coupled with an order of magnitude advantage in machine acquisition cost. SRIM is a somewhat large (30,000 lines of Fortran 77) program designed for uniprocessors; its restructuring for a hypercube provides new lessons in the task of alteri ...

18 Coarse-grained parallelism for hierarchical radiosity using group iterative methods
Thomas A. Funkhouser
August 1996 **Proceedings of the 23rd annual conference on Computer graphics and interactive techniques**
Full text available: pdf(358.69 KB) Additional Information: full citation, references, citings, index terms

19 HW/SW co-design: Instruction set and functional unit synthesis for SIMD processor cores
Nozomu Togawa, Koichi Tachikake, Yuichiro Miyaoka, Masao Yanagisawa, Tatsuo Ohtsuki
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**
Full text available: pdf(161.66 KB) Publisher Site Additional Information: full citation, abstract, references

This paper focuses on SIMD processor synthesis and proposes a SIMD instruction set/functional unit synthesis algorithm. Given an initial assembly code and a timing constraint, the proposed algorithm synthesizes an area-optimized processor core with optimal SIMD functional units. It also synthesizes a SIMD instruction set. The input initial assembly code is assumed to run on a full-resource SIMD processor (virtual processor) which has all the possible SIMD functional units. In our algorithm, we i ...

20 Hardware supported optimization: Generation of permutations for SIMD processors
Alexei Kudriavtsev, Peter Kogge
June 2005 **Proceedings of the 2005 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems**
Full text available: pdf(356.05 KB) Additional Information: full citation, abstract, references, index terms

Short vector (SIMD) instructions are useful in signal processing, multimedia, and scientific applications. They offer higher performance, lower energy consumption, and better resource utilization. However, compilers still do not have good support for SIMD instructions, and often the code has to be written manually in assembly language or using compiler builtin functions. Also, in some applications, higher parallelism could be achieved if compilers inserted permutation instructions that reorder t ...

Keywords: SIMD, permutations

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1 Real-time programmable shading

Anselmo Lastra, Steven Molnar, Marc Olano, Yulan Wang

April 1995 **Proceedings of the 1995 symposium on Interactive 3D graphics**

Full text available: pdf(3.67 MB) Additional Information: full citation, abstract, references, citings, index terms

One of the main techniques used by software renderers to produce stunningly realistic images is programmable shading—executing an arbitrarily complex program to compute the color at each pixel. Thus far, programmable shading has only been available on software rendering systems that run on general-purpose computers. Rendering each image can take from minutes to hours.Parallel rendering engines, on the other hand, have steadily increased in generality and in performance. We ...

2 PixelFlow: the realization

John Eyles, Steven Molnar, John Poulton, Trey Greer, Anselmo Lastra, Nick England, Lee Westover

August 1997 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.54 MB) Additional Information: full citation, references, citings, index terms

Keywords: compositing, deferred shading, object-parallel, rendering, scalable

3 An updated cross-indexed guide to the ray-tracing literature

L. Richard Speer

January 1992 **ACM SIGGRAPH Computer Graphics**, Volume 26 Issue 1

Full text available: pdf(2.94 MB) Additional Information: full citation, index terms

4 14.9 TFLOPS three-dimensional fluid simulation for fusion science with HPF on the Earth Simulator

Hitoshi Sakagami, Hitoshi Murai, Yoshiki Seo, Mitsuo Yokokawa

November 2002 **Proceedings of the 2002 ACM/IEEE conference on Supercomputing**

Full text available: pdf(522.96 KB) Additional Information: full citation, abstract, references, index terms

We succeeded in getting 14.9 TFLOPS performance when running a plasma simulation code IMPACT-3D parallelized with High Performance Fortran on 512 nodes of the Earth Simulator. The theoretical peak performance of the 512 nodes is 32 TFLOPS, which means 45% of the peak performance was obtained with HPF. IMPACT-3D is an implosion analysis code using TVD scheme, which performs three-dimensional compressible and inviscid Eulerian fluid computation with the explicit 5-point stencil scheme for spatial ...

5 An extendable optically interconnected parallel computer

Alastair D. McAulay

November 1986 **Proceedings of 1986 ACM Fall joint computer conference**

Full text available: pdf(722.58 KB) Additional Information: full citation, references, index terms

6 A design analysis of a hybrid technology multithreaded architecture for petaflops scale computation3

Thomas Sterling, Larry Bergman

May 1999 **Proceedings of the 13th international conference on Supercomputing**

Full text available: pdf(1.92 MB) Additional Information: full citation, references, citings, index terms

7 Set operations on polyhedra using binary space partitioning trees
William C. Thibault, Bruce F. Naylor
August 1987 **ACM SIGGRAPH Computer Graphics , Proceedings of the 14th annual conference on Computer graphics and interactive techniques**, Volume 21 Issue 4
Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, references, citings, index terms

We introduce a new representation for polyhedra by showing how Binary Space Partitioning Trees (BSP trees) can be used to represent regular sets. We then show how they may be used in evaluating set operations on polyhedra. The BSP tree is a binary tree representing a recursive partitioning of d-space by (sub-)hyperplanes, for any dimension d. Their previous application to computer graphics has been to organize an arbitrary set of polygons so that a fast solution to the visible surface problem co ...

8 Data modeling and security: An abstract model of three-dimensional spatial data types
Markus Schneider, Brian E. Weinrich
November 2004 **Proceedings of the 12th annual ACM international workshop on Geographic information systems**
Full text available: pdf(208.71 KB) Additional Information: full citation, abstract, references, index terms

Although spatial objects of our world have an intrinsic three-dimensional (3D) nature, <i>3D data modeling</i> and <i>3D data management</i> have so far been neglected in spatial database systems and Geographical Information Systems, which map geometric data mainly to two-dimensional abstractions. But increasingly the third dimension becomes more and more relevant for application domains like pollution control, water supply, soil engineering, urban planning, and aviation. Larg ...

Keywords: 3D spatial data type, GIS, algebra, data model, spatial database

9 Lower bounds for parallel linear programming and other problems
Ketan Mulmuley
May 1994 **Proceedings of the twenty-sixth annual ACM symposium on Theory of computing**
Full text available: pdf(1.42 MB) Additional Information: full citation, references, citings, index terms

10 A shading language on graphics hardware: the pixelflow shading system
Marc Olano, Anselmo Lastra
July 1998 **Proceedings of the 25th annual conference on Computer graphics and interactive techniques**
Full text available: pdf(238.26 KB) Additional Information: full citation, references, citings, index terms

Keywords: procedural shading, real-time image generation, shading language

11 A superscalar 3D graphics engine
Andrew Wolfe, Derek B. Noonburg
November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(1.18 MB) Publisher Site Additional Information: full citation, abstract, references, index terms

3D graphics performance is increasing faster than any other computing application. Almost all PC systems now include 3D graphics accelerators for games, CAD, or visualization applications. Many of the microarchitectural techniques that have been used to enhance the performance of microprocessors can be applied to graphics systems as well. We present an architecture for an out-of-order, superscalar rasterizer for 3D graphics. This allows the concurrent execution of multiple graphics ...

12 Modeling polyhedral solids bounded by multi-curved parametric surfaces
Yehuda E. Kalay
January 1982 **Proceedings of the 19th conference on Design automation**
Full text available: pdf(571.29 KB) Additional Information: full citation, abstract, references, citings, index terms

Since the beginning of geometric modeling as a field of CAD a decade ago, the methods for interactive design of solid objects and interactive design of free-formed surfaces (of degree 3 and higher) were developed along parallel but disjoint strands. One led to the development of techniques for representing and manipulating the shape of polyhedral solids bounded mostly by planes, while the other led to the development of techniques for the mathematical representation of curved surfac ...

13 Pixel-planes 5: a heterogeneous multiprocessor graphics system using processor-enhanced memories

Henry Fuchs, John Poulton, John Eyles, Trey Greer, Jack Goldfeather, David Ellsworth, Steve Molnar, Greg Turk, Brice Tebbs, Laura Israel
July 1989 **ACM SIGGRAPH Computer Graphics , Proceedings of the 16th annual conference on Computer graphics and interactive techniques**, Volume 23 Issue 3
Full text available: pdf(2.01 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper introduces the architecture and initial algorithms for Pixel-Planes 5, a heterogeneous multi-computer designed both for high-speed polygon and sphere rendering (1M Phong-shaded triangles/second) and for supporting algorithm and application research in interactive 3D graphics. Techniques are described for volume rendering at multiple frames per second, font generation directly from conic spline descriptions, and rapid calculation of radiosity form-factors. The hardware consists of up t ...

14 The Quadtree and Related Hierarchical Data Structures
Hanan Samet
June 1984 **ACM Computing Surveys (CSUR)**, Volume 16 Issue 2
Full text available: pdf(4.87 MB) Additional Information: full citation, references, citings, index terms

15 Hardware accelerated rendering of CSG and transparency
Michael Kelley, Kirk Gould, Brent Pease, Stephanie Winner, Alex Yen
July 1994 **Proceedings of the 21st annual conference on Computer graphics and interactive techniques**
Full text available: pdf(465.36 KB) ps(15.00 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes algorithms for implementing accurate rendering of CSG and transparency in a hardware 3D accelerator. The algorithms are based on a hardware architecture which performs front-to-back Z-sorted shading; a multiple-pass algorithm which allows an unlimited number of Z-sorted object layers is also described. The multiple-pass algorithm has been combined with an image partitioning algorithm to improve efficiency, and to improve performance of the resulting hardware implementat ...

Keywords: CSG, deferred shading, image partitioning, scanline, transparency

16 A system model for computer performance evaluation
D. J. Kuck, B. Kumar
March 1976 **Proceedings of the 1976 ACM SIGMETRICS conference on Computer performance modeling measurement and evaluation**
Full text available: pdf(693.61 KB) Additional Information: full citation, abstract, references, citings, index terms

A framework for the study of computer capacity is given by means of a definition of capacity in terms of speeds of various parts of a computer as well as memory size. In addition to these machine parameters, we also include certain parameters of the programs to be run on a given machine. The calculation of theoretical capacity is given for several combinations of processor, memory, and I/O bandwidth for overlapped machines. The tradeoff between primary memory size and I/O bandwidth is discu ...

17 Blend surfaces for set theoretic volume modelling systems
Alan E. Middleditch, Kenneth H. Sears
July 1985 **ACM SIGGRAPH Computer Graphics , Proceedings of the 12th annual conference on Computer graphics and interactive techniques**, Volume 19 Issue 3
Full text available: pdf(3.31 MB) Additional Information: full citation, abstract, references, citings, index terms

Most volume modelling systems are very limited in the complexity of the surfaces which they support. This is satisfactory for basic models of most mechanical components, since the functional surfaces are not usually complex. However, there are often blends between simple base surfaces. This paper presents a technique appropriate for blend definition and profile control. A discussion of blend conics is used to develop analogous surfaces for use in typical volume modelling systems. These surfaces ...

Keywords: computer aided design, curved surfaces, ray tracing, volume modelling

18 Merging BSP trees yields polyhedral set operations
Bruce Naylor, John Amanatides, William Thibault
September 1990 **ACM SIGGRAPH Computer Graphics , Proceedings of the 17th annual conference on Computer graphics and interactive techniques**, Volume 24 Issue 4
Full text available: pdf(1.04 MB) Additional Information: full citation, abstract, references, citings, index terms

BSP trees have been shown to provide an effective representation of polyhedra through the use of spatial subdivision, and are an alternative to the topologically based b-reps. While bsp tree algorithms are known for a number of important operations, such as rendering, no previous work on bsp trees has provided the capability of performing boolean set operations between two objects represented by bsp trees, i.e. there has been no closed boolean algebra when using bsp trees. This paper presents th ...

19 A perturbation scheme for spherical arrangements with application to molecular modeling
Dan Halperin, Christian R. Shelton
August 1997 **Proceedings of the thirteenth annual symposium on Computational geometry**
Full text available: pdf(1.31 MB) Additional Information: full citation, references, citings, index terms

20 Numerical issues and robustness: Controlled perturbation for arrangements of circles
Dan Halperin, Eran Leiserowitz
June 2003 **Proceedings of the nineteenth annual symposium on Computational geometry**
Full text available: pdf(606.47 KB) Additional Information: full citation, abstract, references, index terms

Given a collection *C* of circles in the plane, we wish to construct the arrangement *A(C)* (namely the subdivision of the plane into vertices, edges and faces induced by *C*) using floating point arithmetic. We present an efficient scheme, controlled perturbation, that perturbs the circles in *C* slightly to form a collection *C'*, so that all the predicates that arise in the construction of *A(C')* are computed accurately and *A(C')* is degeneracy free.We int ...

Keywords: arrangements, perturbation, robustness

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L3	9	(array adj processor or processor adj array) and (surface adj region?)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L4	1315356	region	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L5	130	(array adj processor or processor adj array) same region	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L6	631169	buffer or buffers	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L7	10	((array adj processor or processor adj array) same region) same (buffer or buffers)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L8	3609	surface adj analysis	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L9	0	(array adj processor or processor adj array) same (surface adj analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L10	0	(array adj processor or processor adj array) and (surface adj analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L11	37887	surface with analysis	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L12	1	(array adj processor or processor adj array) same (surface with analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L13	41	(array adj processor or processor adj array) and (surface with analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26

L14	11328	address adj generator	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L15	32	(array adj processor or processor adj array) same (address adj generator)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L16	6	(buffer or buffers) same ((array adj processor or processor adj array) same (address adj generator))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L17	93	((address adj generator) same (buffer or buffers)) and (array adj processor or processor adj array)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L18	0	(((address adj generator) same (buffer or buffers)) and (array adj processor or processor adj array)) and (surface adj analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L19	17751	image adj analysis	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L20	25	(address adj generator) same (buffer or buffers) and (image adj analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L21	576	array.ab. adj processor.ab. or processor.ab. adj array.ab.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L22	0	(buffer or buffers) and (surface adj analysis) and (address adj generator) and (array.ab. adj processor.ab. or processor.ab. adj array.ab.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L23	0	((array adj processor or processor adj array) and (surface with analysis)) and (address adj generator)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L24	93	(array adj processor or processor adj array) and region and (address adj generator) and (buffer or buffers)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L25	483	711/200.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L26	165	712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L27	77	712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26

L28	2	(array adj processor or processor adj array) and (surface adj region?) and 711/200.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L29	0	(array adj processor or processor adj array) and (surface adj region?) and 712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L30	0	(array adj processor or processor adj array) and (surface adj region?) and 712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L31	0	(array adj processor or processor adj array) and (surface adj analysis) and 711/200.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L32	0	(array adj processor or processor adj array) and (surface adj analysis) and 712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L33	0	(array adj processor or processor adj array) and (surface adj analysis) and 712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L34	0	711/200.ccls. and 712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L35	0	711/200.ccls. and 712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L36	1	(array adj processor or processor adj array) and (address adj generator) and 712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L37	3	address adj generator same concurrent adj processing	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L38	42	address adj generator and concurrent adj processing	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L39	39	(address adj generator and concurrent adj processing) not (address adj generator same concurrent adj processing)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L40	4440352	surface	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L41	9	((address adj generator and concurrent adj processing) not (address adj generator same concurrent adj processing)) and surface	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26

L42	30073	parallel adj process$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L43	11328	address adj generator	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L44	75	(parallel adj process$3) same (address adj generator)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L45	9	surface and ((parallel adj process$3) same (address adj generator))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L46	3977	array adj processor or processor adj array	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L47	11328	address adj generator	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L48	3165	sisd or simd or mimd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L49	24830	parallel adj processing or parallel adj processor	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L50	232	(array adj processor or processor adj array) and (address adj generator)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L51	79	(sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L52	67	(parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L53	63	(address adj generator) same (parallel adj processing or parallel adj processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L54	6	((parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))) and ((address adj generator) same (parallel adj processing or parallel adj processor))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L55	113	345/571.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26

L56	175	345/572.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L57	60	345/573.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L58	334	345/571.ccls. or 345/572.ccls. or 345/573.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L59	4	((array adj processor or processor adj array) and (address adj generator)) and (345/571.ccls. or 345/572.ccls. or 345/573.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L60	23	(parallel adj processing or parallel adj processor) and (345/571.ccls. or 345/572.ccls. or 345/573. ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L61	6	(array adj processor or processor adj array) and (array adj processor or processor adj array) and (345/571.ccls. or 345/572.ccls. or 345/573.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L62	232	(array adj processor or processor adj array) and (address adj generator)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L63	24830	parallel adj processing or parallel adj processor	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L64	24305	parallel adj processing or parallel adj processor?	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L65	67	(parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L66	123	((array adj processor or processor adj array) and (address adj generator)) and (parallel adj processing or parallel adj processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L67	67	((parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))) and (((array adj processor or processor adj array) and (address adj generator)) and (parallel adj processing or parallel adj processor))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L68	269	345/505.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26

L69	298	345/506.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L70	506	345/505.ccls. or 345/506.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L71	3	(((parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))) and (((array adj processor or processor adj array) and (address adj generator)) and (parallel adj processing or parallel adj processor))) and (345/505.ccls. or 345/506.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L72	8	(((array adj processor or processor adj array) and (address adj generator)) and (parallel adj processing or parallel adj processor)) and (345/505.ccls. or 345/506.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L73	551	711/168.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L74	483	711/200.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L75	165	712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L76	77	712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L77	113	345/571.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L78	175	345/572.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:26
L79	60	345/573.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L80	269	345/505.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L81	298	345/506.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27

L82	67	(parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L83	3977	array adj processor or processor adj array	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L84	10965	surface adj region?	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L85	1315356	region	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L86	130	(array adj processor or processor adj array) same region	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L87	631169	buffer or buffers	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L88	3609	surface adj analysis	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L89	0	(array adj processor or processor adj array) same (surface adj analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L90	0	(array adj processor or processor adj array) and (surface adj analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L91	37887	surface with analysis	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L92	11328	address adj generator	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L93	93	((address adj generator) same (buffer or buffers)) and (array adj processor or processor adj array)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L94	0	(((address adj generator) same (buffer or buffers)) and (array adj processor or processor adj array)) and (surface adj analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L95	17751	image adj analysis	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27

L96	576	array.ab. adj processor.ab. or processor.ab. adj array.ab.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L97	0	(buffer or buffers) and (surface adj analysis) and (address adj generator) and (array.ab. adj processor.ab. or processor.ab. adj array.ab.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L98	0	((array adj processor or processor adj array) and (surface with analysis)) and (address adj generator)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L99	93	(array adj processor or processor adj array) and region and (address adj generator) and (buffer or buffers)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L100	483	711/200.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L101	165	712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L102	77	712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L103	2	(array adj processor or processor adj array) and (surface adj region?) and 711/200.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L104	0	(array adj processor or processor adj array) and (surface adj region?) and 712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L105	0	(array adj processor or processor adj array) and (surface adj region?) and 712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L106	0	(array adj processor or processor adj array) and (surface adj analysis) and 711/200.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L107	0	(array adj processor or processor adj array) and (surface adj analysis) and 712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L108	0	(array adj processor or processor adj array) and (surface adj analysis) and 712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L109	0	711/200.ccls. and 712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27

L110	0	711/200.ccls. and 712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L111	42	address adj generator and concurrent adj processing	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L112	39	(address adj generator and concurrent adj processing) not (address adj generator same concurrent adj processing)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L113	4440352	surface	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L114	30073	parallel adj process$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L115	11328	address adj generator	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L116	75	(parallel adj process$3) same (address adj generator)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L117	3977	array adj processor or processor adj array	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L118	11328	address adj generator	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L119	3165	sisd or simd or mimd	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L120	24830	parallel adj processing or parallel adj processor	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L121	232	(array adj processor or processor adj array) and (address adj generator)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L122	79	(sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L123	67	(parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27

L124	63	(address adj generator) same (parallel adj processing or parallel adj processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L125	113	345/571.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L126	175	345/572.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L127	60	345/573.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L128	334	345/571.ccls. or 345/572.ccls. or 345/573.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L129	232	(array adj processor or processor adj array) and (address adj generator)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L130	24830	parallel adj processing or parallel adj processor	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L131	24305	parallel adj processing or parallel adj processor?	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L132	67	(parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L133	123	((array adj processor or processor adj array) and (address adj generator)) and (parallel adj processing or parallel adj processor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L134	67	((parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))) and (((array adj processor or processor adj array) and (address adj generator)) and (parallel adj processing or parallel adj processor))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L135	269	345/505.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L136	298	345/506.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27

L137	506	345/505.ccls. or 345/506.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L138	551	711/168.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L139	483	711/200.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L140	165	712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L141	77	712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L142	113	345/571.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L143	175	345/572.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L144	60	345/573.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L145	269	345/505.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L146	298	345/506.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L147	67	(parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L148	1	(array adj processor or processor adj array) same (surface with analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L149	1	(array adj processor or processor adj array) and (address adj generator) and 712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L150	9	(array adj processor or processor adj array) and (surface adj region?)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27

L151	10	((array adj processor or processor adj array) same region) same (buffer or buffers)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L152	41	(array adj processor or processor adj array) and (surface with analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L153	32	(array adj processor or processor adj array) same (address adj generator)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L154	6	(buffer or buffers) same ((array adj processor or processor adj array) same (address adj generator))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L155	25	(address adj generator) same (buffer or buffers) and (image adj analysis)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L156	3	address adj generator same concurrent adj processing	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L157	9	((address adj generator and concurrent adj processing) not (address adj generator same concurrent adj processing)) and surface	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L158	9	surface and ((parallel adj process$3) same (address adj generator))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L159	6	((parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))) and ((address adj generator) same (parallel adj processing or parallel adj processor))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L160	4	((array adj processor or processor adj array) and (address adj generator)) and (345/571.ccls. or 345/572.ccls. or 345/573.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L161	23	(parallel adj processing or parallel adj processor) and (345/571.ccls. or 345/572.ccls. or 345/573. ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L162	6	(array adj processor or processor adj array) and (array adj processor or processor adj array) and (345/571.ccls. or 345/572.ccls. or 345/573.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L163	3	(((parallel adj processing or parallel adj processor) and ((sisd or simd or mimd) and ((array adj processor or processor adj array) and (address adj generator)))) and (((array adj processor or processor adj array) and (address adj generator)) and (parallel adj processing or parallel adj processor))) and (345/505.ccls. or 345/506.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27

L164	8	(((array adj processor or processor adj array) and (address adj generator)) and (parallel adj processing or parallel adj processor)) and (345/505.ccls. or 345/506.ccls.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L165	50	("6631457" "4521874" "5276826" "4809156" "4893234" "5987574" "6051772" "5588138" "4386410" "4412294" "4802118" "5469559" "5809254" "5719996" "5512819" "5999911" "5187783" "5289574" "6442663" "4269281" "4298936" "4385352" "4400768" "4408271" "4435756" "4459662" "4463422" "4468753" "4503429" "4541094" "4553203" "4593350" "4594655" "4599689" "4611310" "4757466" "4811201" "4812847" "4819154" "4939727" "5218709" "5257394" "5261111" "5268856" "5287452" "5325491" "5361367" "5369773" "5438670" "5490258").pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L166	3	(US-6631457-$ or US-5361367-$ or US-4298936-$).did.	USPAT	OR	OFF	2005/07/09 17:27
L167	3977	(array adj processor) or (processor adj array)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L168	11268	(surface adj region?) or ((2D adj region) or (2D-region)) or ((3D adj region) or (3D-region))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L169	24	L167 and L168	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L170	30207	address adj generat$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L171	2	L169 and L170	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L172	11112	((surface adj region?) or ((2D adj region) or (2D-region)) or ((3D adj region) or (3D-region)) with (size or sizing) with (reduc$3 or adjust$3 or modif$7))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L173	453636	((size or sizing) with (reduc$3 or adjust$3 or modif$7))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L174	23	L168 with L173	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L175	10434349	@ad<"19991101"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27

L176	46	L169 or L174	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L177	24	L175 and L176	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L178	41941	size with (correspond or corresponds or corresponding)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L179	3	L168 with L178	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L180	483	711/200.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L181	551	711/168.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L182	165	712/10.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L183	354	712/11.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L184	77	712/17.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L185	113	345/571.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L186	175	345/572.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L187	60	345/573.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L188	269	345/505.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L189	298	345/506.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27

L190	1026	L180 or L181	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L191	541	L182 or L183 or L184	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L192	829	L185 or L186 or L187 or L188 or L189	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L193	2	L169 and L190	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L194	1	L169 and L191	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L195	1	L169 and L192	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L196	2	instruction with L168	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L197	14	US-4891751-$.DID. OR US-4975843-$.DID. OR US-5038386-$.DID. OR US-6266733-$.DID. OR US-6532017-$.DID. OR US-4811210-$.DID. OR US-4907148-$.DID. OR US-5794016-$.DID. OR US-5193202-$.DID. OR US-5692210-$.DID. OR US-5781195-$.DID. OR US-6460127-$.DID. OR US-5524223-$.DID. OR US-4051551-$.DID.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L198	0	L169 and L197	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L199	192171	"345"/("606,607,608,609,610").ccls.	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L200	192171	"345"/("501,502,503,504,505,506,522").ccls.	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L201	192171	L199 and L200	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L202	2999428	surface or region	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L203	4126	first adj operand wiht second adj operand	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L204	1727	first adj operand with second adj operand	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L205	646	(first adj operand with second adj operand) with instruction	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L206	91	L202 and L205	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27

L207	14	L201 and L206	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L208	2953403	@ad<"19991101"	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L209	13	L207 and L208	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L210	15	surface and L205	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L211	112906	L201 and surface	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L212	2	L205 and L211	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L213	95685	"712"/("20,21,22").ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L214	210853	"345"/("606,607,608,609,610").ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L215	210853	"345"/("501,502,503,504,505,506,519,520,522"). ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L216	210853	L214 or L215	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L217	295351	L213 or L216	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L218	10965	surface adj region?	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L219	777	L217 and L218	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L220	11112	((surface adj region?) or ((2D adj region) or (2D-region)) or ((3D adj region) or (3D-region)) with (size or sizing) with (reduc$3 or adjust$3 or modif$7))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L221	804	L217 and L220	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L222	646	(first adj operand with second adj operand) with instruction	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27

L223	0	(L219 or L221) and L222	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L224	209	L217 and L222	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L225	0	L218 and L224	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L226	660892	region?	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L227	21	L224 and L226	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L228	2953403	@ad<"19991101"	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L229	16	L227 and L228	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L230	562	L218 and L216	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L231	0	L222 and L230	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L232	19	(first adj operand with second adj operand) with instruction with parallel	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L233	562	L215 and L218	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L234	2450	simd	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L235	1	L233 and L234	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L236	14	("4051551" | "4811210" | "4891751" | "4907148" | "4975843" | "5038386" | "5193202" | "5524223" | "5692210" | "5781195" | "5794016" | "6266733" | "6460127" | "6532017").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/09 17:27
L237	29754	operand	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L238	2690	first adj operand and second adj operand	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L239	0	L236 and L238	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27

L240	5	L236 and L237	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L241	29754	operand	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L242	2	"5170347".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L243	0	L242 and L241	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L244	2	"5170347".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L245	2543116	parallel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L246	2	L242 and L245	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L247	0	((first adj operand with second adj operand) with instruction) same parallel same region	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L248	8	((first adj operand with second adj operand) with instruction) same parallel same area	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L249	2953403	@ad<"19991101"	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L250	4	L248 and L249	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L251	210853	"345"/("501,502,503,504,505,506,519,520,522"). ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L252	27	712/22.ccls. and L251	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27

L253	20	L249 and L252	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L254	11	L241 and L253	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L255	11	L245 and L254	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L256	114917	L251 and surface	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L257	510	L251 and (surface adj data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 17:27
L258	48	((first adj operand with second adj operand) with instruction) same parallel	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L259	0	L257 and L258	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L260	646	((first adj operand with second adj operand) with instruction)	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L261	0	L257 and L260	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L262	646	((first adj operand with second adj operand) with instruction)	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L263	657	operand with instruction with parallel	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L264	1	L257 and L263	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L265	1412	processor adj array	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L266	2450	simd	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L267	374	L251 and L266	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L268	117	L267 and surface	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L269	4	L263 and L268	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L270	370	L265 and surface	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L271	0	L260 and L270	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27

L272	22	L263 and L270	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L273	21	L249 and L272	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L274	6030	surface adj data	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L275	1	L267 and L274	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L276	93	(array adj processor or processor adj array) and region and (address adj generator) and (buffer or buffers)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L277	646	(first adj operand with second adj operand) with instruction	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L278	0	L276 and L277	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L279	0	L277 and surface adj region	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L280	15	L277 and surface	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L281	10434349	@ad<"19991101"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L282	11	L280 and L281	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L283	19	(first adj operand with second adj operand) with instruction with parallel	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L284	0	L276 and L283	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L285	4	L283 and L280	US-PGPUB; USPAT	OR	ON	2005/07/09 17:27
L286	2775	SIMD	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27
L287	2	L282 and L286	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/07/09 17:27

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"5170347".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:22
L2	29754	operand	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:19
L3	0	1 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:19
L4	2543116	parallel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:22
L5	2	1 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:22
L7	0	((first adj operand with second adj operand) with instruction) same parallel same region	US-PGPUB; USPAT	OR	ON	2005/07/09 16:25
L8	8	((first adj operand with second adj operand) with instruction) same parallel same area	US-PGPUB; USPAT	OR	ON	2005/07/09 16:48
L9	2953403	@ad<"19991101"	US-PGPUB; USPAT	OR	ON	2005/07/09 16:26
L10	4	8 and 9	US-PGPUB; USPAT	OR	ON	2005/07/09 16:26
L11	210853	"345"/("501,502,503,504,505,506,519,520,522"). ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:48
L12	27	712/22.ccls. and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:29
L13	20	9 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:29
L14	11	2 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:29

L15	11	4 and 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:29
L16	114917	11 and surface	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:48
L17	510	11 and (surface adj data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/09 16:48
L18	48	((first adj operand with second adj operand) with instruction) same parallel	US-PGPUB; USPAT	OR	ON	2005/07/09 16:49
L19	0	17 and 18	US-PGPUB; USPAT	OR	ON	2005/07/09 16:49
L20	646	((first adj operand with second adj operand) with instruction)	US-PGPUB; USPAT	OR	ON	2005/07/09 16:49
L21	0	17 and 20	US-PGPUB; USPAT	OR	ON	2005/07/09 16:49
L22	646	((first adj operand with second adj operand) with instruction)	US-PGPUB; USPAT	OR	ON	2005/07/09 16:49
L23	657	operand with instruction with parallel	US-PGPUB; USPAT	OR	ON	2005/07/09 16:50
L24	1	17 and 23	US-PGPUB; USPAT	OR	ON	2005/07/09 16:50
L25	1412	processor adj array	US-PGPUB; USPAT	OR	ON	2005/07/09 16:50
L26	2450	simd	US-PGPUB; USPAT	OR	ON	2005/07/09 16:50
L27	374	11 and 26	US-PGPUB; USPAT	OR	ON	2005/07/09 16:50
L28	117	27 and surface	US-PGPUB; USPAT	OR	ON	2005/07/09 16:50
L29	4	23 and 28	US-PGPUB; USPAT	OR	ON	2005/07/09 16:53
L30	370	25 and surface	US-PGPUB; USPAT	OR	ON	2005/07/09 16:53
L31	0	20 and 30	US-PGPUB; USPAT	OR	ON	2005/07/09 16:53
L32	22	23 and 30	US-PGPUB; USPAT	OR	ON	2005/07/09 16:53
L33	21	9 and 32	US-PGPUB; USPAT	OR	ON	2005/07/09 16:56
L34	6030	surface adj data	US-PGPUB; USPAT	OR	ON	2005/07/09 16:56
L35	1	27 and 34	US-PGPUB; USPAT	OR	ON	2005/07/09 16:56